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CLAIMS

1. A self-refresh transition system for a DRAM device having a plurality of rows of memory cells, the self-refresh transition system comprising:

a transitional refresh controller receptive of a refresh signal and a self-refresh transition signal, the refresh signal indicating when a row is being refreshed and the self-refresh transition signal indicating when a computing system directs the DRAM device to transition between a self-refresh mode and an operational mode, the transitional refresh controller initiating a refresh of at least one row of memory cells when the self-refresh exit signal indicates the computing system is directing the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed.

2. The self-refresh transition system of claim 1 wherein the transitional refresh controller initiates a refresh of at least one row of memory cells when the self-refresh transition signal indicates the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed before transitioning between the self-refresh mode and the operational mode.

3. The self-refresh transition system of claim 1 wherein the transitional refresh controller initiates a refresh of at least one row of memory cells when the computing system directs the DRAM device to transition from the self-refresh mode to the operational mode.

4. The self-refresh transition system of claim 1 wherein the transitional refresh controller initiates a refresh of at least one row of memory cells when the computing system directs the DRAM device to transition from the operational mode to the self-refresh mode.

5. The self-refresh transition system of claim 1 wherein the transitional refresh controller initiates a refresh of at least one row of memory cells when the computing system directs the DRAM device to transition both from the operational mode to the self-refresh mode and from the self-refresh mode to the operational mode.

6. The self-refresh transition system of claim 1 wherein the transitional refresh controller initiates a refresh of a single row of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

7. The self-refresh transition system of claim 1 wherein the transitional refresh controller initiates a refresh of multiple rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

8. The self-refresh transition system of claim 1 wherein the transitional refresh controller initiates a refresh of all rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

9. The self-refresh transition system of claim 1 wherein the transitional refresh controller, when the self-refresh exit signal indicates the computing system is directing the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed, disengages a self-refresh clock during refresh of at least one row of memory cells.

10. A self-refresh transition system for a DRAM device having a plurality of rows of memory cells, the self-refresh transition system comprising:

a transitional refresh controller receptive of a refresh signal and a self-refresh transition signal, the refresh signal indicating when a row is being refreshed and the self-refresh transition signal indicating when a computing system directs the DRAM device to transition between a self-refresh mode and an operational mode, the transitional refresh controller

disengaging a self-refresh clock and initiating a refresh of at least one row of memory cells when the self-refresh exit signal indicates the computing system is directing the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed, before transitioning between the self-refresh mode and the operational mode.

11. The self-refresh transition system of claim 10 wherein the transitional refresh controller initiates a refresh of at least one row of memory cells when the computing system directs the DRAM device to transition from the operational mode to the self-refresh mode.

12. The self-refresh transition system of claim 10 wherein the transitional refresh controller initiates a refresh of at least one row of memory cells when the computing system directs the DRAM device to transition from the self-refresh mode to the operational mode.

13. The self-refresh transition system of claim 10 wherein the transitional refresh controller initiates a refresh of at least one row of memory cells when the computing system directs the DRAM device to transition both from the operational mode to the self-refresh mode and from the self-refresh mode to the operational mode.

14. The self-refresh transition system of claim 10 wherein the transitional refresh controller initiates a refresh of a single row of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

15. The self-refresh transition system of claim 10 wherein the transitional refresh controller initiates a refresh of multiple rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

16. The self-refresh transition system of claim 10 wherein the transitional refresh controller initiates a refresh of all rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

17. A self-refresh control system directing a DRAM device having a plurality of rows of memory cells during a self-refresh mode, the self-refresh control system comprising:

a self-refresh clock issuing a self-refresh clock signal;

a row refreshing circuit, receptive of the self-refresh clock signal, the row refreshing circuit directing a refresh of a row of memory cells in response to the self-refresh clock signal; and

a transitional refresh controller receptive of a refresh signal and a self-refresh transition signal, the refresh signal indicating when a row is being refreshed and the self-refresh transition signal indicating when a computing system directs the DRAM device to transition between a self-refresh mode and an operational mode, the transitional refresh controller initiating a refresh of at least one row of memory cells when the self-refresh exit signal indicates the computing system is directing the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed.

18. The self-refresh control system of claim 17 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the self-refresh exit signal indicates the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed, before transitioning between the self-refresh mode and the operational mode.

19. The self-refresh control system of claim 17 wherein the transitional refresh controller directs the row refreshing circuit to a refresh at least one row of memory cells when the computing system directs the DRAM device to transition from the operational mode to the self-refresh mode.

20. The self-refresh control system of claim 17 wherein the transitional refresh controller directs the row refreshing circuit to a refresh at least one row of memory cells when the computing system directs the DRAM device to transition from the self-refresh mode to the operational mode.

21. The self-refresh control system of claim 17 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the computing system directs the DRAM device to transition both from the operational mode to the self-refresh mode and from the self-refresh mode to the operational mode.

22. The self-refresh control system of claim 17 wherein the transitional refresh controller directs the row refreshing circuit to refresh a single row of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

23. The self-refresh control system of claim 17 wherein the transitional refresh controller directs the row refreshing circuit to refresh multiple rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

24. The self-refresh control system of claim 17 wherein the transitional refresh controller directs the row refreshing circuit to refresh all rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

25. The self-refresh control system of claim 17 wherein the transitional refresh controller disengages the self-refresh clock during refresh of at least one row of memory cells when the self-refresh exit signal indicates the computing system is directing the DRAM device to

transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed.

26. A DRAM device comprising:

a plurality of rows of DRAM memory cells;

a row addressing system operably connected to the DRAM array, the row addressing system responsive to a row address signal by accessing a row in the DRAM array corresponding to the row address signal;

a self-refresh clock issuing a self-refresh clock signal;

a row refreshing circuit, operably connected with the row addressing system and the plurality of rows of DRAM memory cells, the row refreshing circuit directing a refresh of at least one row of memory cells in response to one of the self-refresh clock signal;

a refresh signal indicating when a row of memory cells is being refreshed by the row refreshing circuit;

a self-refresh transition signal indicating when a computing system is directing the DRAM device to transition between self-refresh mode and an operational mode; and

a transitional refresh controller receptive of a refresh signal and a self-refresh transition signal, the refresh signal indicating when a row is being refreshed and the self-refresh transition signal indicating when a computing system directs the DRAM device to transition between a self-refresh mode and an operational mode, the transitional refresh controller initiating a refresh of at least one row of memory cells when the self-refresh exit signal indicates the computing system is directing the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed.

27. The DRAM device of claim 26 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the self-refresh exit signal indicates the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode and the refresh signal does not indicate a row is

presently being refreshed before transitioning between the self-refresh mode and the operational mode.

28. The DRAM device of claim 26 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the computing system directs the DRAM device to transition from the self-refresh mode to the operational mode.

29. The DRAM device of claim 26 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the computing system directs the DRAM device to transition from the operational mode to the self-refresh mode.

30. The DRAM device of claim 26 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the computing system directs the DRAM device to transition both from the operational mode to the self-refresh mode and from the self-refresh mode to the operational mode.

31. The DRAM device of claim 26 wherein the transitional refresh controller initiates a refresh of a single row of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

32. The DRAM device of claim 26 wherein the transitional refresh controller initiates a refresh of multiple rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

33. The DRAM device of claim 26 wherein the transitional refresh controller initiates a refresh of all rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

34. The DRAM device of claim 26 wherein the transitional refresh controller disengages the self-refresh clock during refresh of at least one row of memory cells when the self-refresh exit signal indicates the computing system is directing the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed.

35. A computer system, comprising:

a processor;

an input device, operably connected to the processor, allowing data to be entered into the computer system;

an output device, operably connected to the processor, allowing data to be output from the computer system; and

a system memory operably connected to the processor, comprising a plurality of DRAM devices, the DRAM devices comprising a row addressing system operably connected to the DRAM array, the row addressing system responsive to a row address signal by accessing a row in the DRAM array corresponding to the row address signal; a self-refresh clock issuing a self-refresh clock signal; a row refreshing circuit, operably connected with the row addressing system and the plurality of rows of DRAM memory cells, the row refreshing circuit directing a refresh of at least one row of memory cells in response to one of the self-refresh clock signal and an immediate refresh signal; and a transitional refresh controller receptive of a refresh signal and a self-refresh transition signal, the refresh signal indicating when a row is being refreshed and the self-refresh transition signal indicating when a computing system directs the DRAM device to transition between a self-refresh mode and an operational mode, the transitional refresh controller initiating a refresh of at least one row of memory cells when the self-refresh exit signal indicates the computing system is directing the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed; and

a data path coupled to an external data terminal of the DRAM array.

36. The computer system of claim 35 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the self-refresh exit signal indicates the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode, and the refresh signal does not indicate a row is presently being refreshed before transitioning between the self-refresh mode and the operational mode.

37. The computer system of claim 35 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the computing system directs the DRAM device to transition from the self-refresh mode to the operational mode.

38. The computer system of claim 35 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the computing system directs the DRAM device to transition from the operational mode to the self-refresh mode.

39. The computer system of claim 35 wherein the transitional refresh controller directs the row refreshing circuit to refresh at least one row of memory cells when the computing system directs the DRAM device to transition both from the operational mode to the self-refresh mode and from the self-refresh mode to the operational mode.

40. The computer system of claim 35 wherein the transitional refresh controller initiates a refresh of a single row of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

41. The computer system of claim 35 wherein the transitional refresh controller initiates a refresh of multiple rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

42. The computer system of claim 35 wherein the transitional refresh controller initiates a refresh of all rows of memory cells when the computing system directs the DRAM device to transition between the self-refresh mode and the operational mode.

43. The computer system of claim 35 wherein the transitional refresh controller disengages the self-refresh clock during refresh of at least one row of memory cells when the self-refresh exit signal indicates the computing system is directing the DRAM device to transition between the self-refresh mode and the operational mode and the refresh signal does not indicate a row is presently being refreshed.

44. A method for transitioning a DRAM device having a plurality of rows of memory cells between self-refreshing and operating, comprising:

detecting when a row is being refreshed;

detecting when a computing system directs the DRAM device to transition between refreshing itself and operating; and

initiating a refresh of at least one row of memory cells upon detecting the computing system is directing the DRAM device to transition between self-refreshing and operating when no row is being refreshed.

45. The method of claim 44 wherein refreshing of at least one row of memory cells is completed before the DRAM device transitions between self-refreshing and operating.

46. The method of claim 44 wherein at least one row of memory cells is refreshed when the computing system directs the DRAM device to transition from self-refreshing to operating.

47. The method of claim 44 wherein at least one row of memory cells is refreshed when the computing system directs the DRAM device to transition operating to self-refreshing.

48. The method of claim 44 wherein at least one row of memory cells is refreshed when the computing system directs the DRAM device to transition both from operating to self-refreshing and from self-refreshing to operating.

49. The method of claim 44 wherein a single row of memory cells is refreshed when the computing system directs the DRAM device to transition between self-refreshing and operating.

50. The method of claim 44 wherein multiple rows of memory cells are refreshed when the computing system directs the DRAM device to transition between self-refreshing and operating.

51. The method of claim 44 wherein all rows of memory cells are refreshed when the computing system directs the DRAM device to transition between self-refreshing and operating.

52. The method of claim 44 wherein upon detecting the computing system is directing the DRAM device to transition between self-refreshing and operating and no row is being refreshed, self-refresh clocking is disengaged.

53. A method for transitioning a DRAM device between self-refreshing and operating, the DRAM device having a plurality of rows of memory cells, the method comprising:

detecting when a row is being refreshed;

detecting when a computing system directs the DRAM device to transition between refreshing itself and operating;

initiating a refresh of at least one row of memory cells upon detecting the computing system is directing the DRAM device to transition between self-refreshing and operating and no row is being refreshed before transitioning between self-refreshing and operating.

54. The method of claim 53 wherein at least one row of memory cells is refreshed when the computing system directs the DRAM device to transition from self-refreshing to operating.

55. The method of claim 53 wherein at least one row of memory cells is refreshed when the computing system directs the DRAM device to transition from operating to self-refreshing.

56. The method of claim 53 wherein at least one row of memory cells is refreshed when the computing system directs the DRAM device to transition both from operating to self-refreshing and from self-refreshing to operating.

57. The method of claim 53 wherein a single row of memory cells is refreshed when the computing system directs the DRAM device to transition between self-refreshing and operating.

58. The method of claim 53 wherein multiple rows of memory cells are refreshed when the computing system directs the DRAM device to transition between self-refreshing and operating.

59. The method of claim 53 wherein all rows of memory cells are refreshed when the computing system directs the DRAM device to transition between self-refreshing and operating.

60. The method of claim 53 wherein upon detecting the computing system is directing the DRAM device to transition between self-refreshing and operating and no row is being refreshed, self-refresh clocking is disengaged.